

**Optimized Modeling Solution to Predict Board Warpage/Localized Stresses:** Higher-performance and lower-power hardware is needed to process fast-growing generative AI (GenAI) workloads such as Large Language Models (LLMs). These devices require more silicon to be integrated into a single package, along with more chip-to-chip interconnects among the packages on a printed circuit board. This means boards are being designed with ever-smaller features, including copper traces with finer lines and spacings, and higher-aspect-ratio vias between metal layers. With these smaller features, identifying key risks such as overall board warpage and localized stress on fine features like traces and vias, is essential to the viability of future hardware.

In this work, [Groq](https://groq.com/) expands on using finite element analysis (FEA) simulations to develop a comprehensive modeling solution. This approach can be used to both evaluate and mitigate risks during board assembly. The researchers studied the advantages and drawbacks of three different modeling approaches to understand global warpage behavior – rule-of-mixture, trace mapping, and full reinforcement modeling. They concluded that an optimal modeling methodology requires a hybrid approach to balance accuracy and computational time. Their proposed warpage-modeling methodology has great accuracy against measurement data for risk-location prediction. Groq also will talk about the importance of other issues – part-to-part manufacturing variations, repeatability testing during temperature cycling, and stress-free temperature identification – that can impact board-level warpage predictions. Moreover, Groq’s proposed methodology also reveals high risk locations for millions of fine feature traces and vias embedded in the board, enabling a thorough understanding of board behavior during the assembly process.

The images above are results of their simulations showing the highest localized stresses on both traces and vias:

* The top left image is a view of localized trace stress in a board; the top right image is a zoomed-in view showing that stress on a trace.
* The bottom left image is a view of localized via stress in a board; the bottom right image is a zoomed-in view showing that stress on a via.

**(Paper 24.6, “*Optimized Simulation Methodology of Warpage and Localized Stress Hotspot Prediction for Assembly Risk Assessment*,” Z. Yang et al, Groq Inc./Ansys)**